WHAT IS CLAIMED IS:

1. A power semiconductor package, comprising:

a bottom leadframe having a bottom plate portion and at least one first terminal extending from the bottom plate portion;

at least one second terminal being co-planar with the first terminal;

a semiconductor power MOSFET die having a bottom surface defining a drain connection and a top surface on which a first metalized region defining a source and a second metalized region defining a gate are disposed, the bottom surface being coupled to the bottom plate of the leadframe such that the first terminal is electrically connected to the drain;

a copper plate coupled to and spanning a substantial part of the first metalized region defining the source connection; and

at least one beam portion being sized and shaped to couple the copper plate portion to the at least one second terminal such that it is electrically coupled to the source.

2. The power semiconductor package of claim 1, further comprising a wire bond coupling the gate to a third terminal.

3. The power semiconductor package of claim 1, further comprising a layer of curable conductive material disposed between the copper plate and the first metalized region such that the copper plate portion is firmly coupled to the source.

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4. The power semiconductor package of claim 1, wherein the copper plate includes a top surface and a bottom surface, the bottom surface having downwardly directed projections extending towards the source.

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5. The power semiconductor package of claim 1, wherein the MOSFET die includes a gate bus extending over portions of the source, the copper plate covering substantially all of the gate bus.

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6. The power semiconductor package of claim 1, wherein the MOSFET die includes a gate bus extending over portions of the source, further comprising a nitride layer substantially covering at least a portion of the gate bus, the copper plate being electrically insulated from the gate bus via the nitride layer.

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7. The power semiconductor package of claim 6, further comprising a layer of curable conductive material disposed between the copper plate and the source.

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8. The power semiconductor package of claim 7, wherein the nitride layer electrically insulates the gate bus from the curable conductive material.

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9. The power semiconductor package of claim 8, wherein the curable conductive material is silver filled epoxy.

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10. The power semiconductor package of claim 1, wherein the at least one beam portion extends from a lateral edge of the copper plate and is coupled to the at least one second terminal at a distal end.

11. The power semiconductor package of claim 10, further comprising a layer of curable conductive material disposed between the distal end of the beam portion and the at least one second terminal.

12. The power semiconductor package of claim 10, wherein the at least one second terminal is integral with the at least one beam portion.

13. The power semiconductor package of claim 10, wherein the beam portion is a single member extending from the lateral edge of the copper plate to the at least one second terminal.

14. The power semiconductor package of claim 10, comprising at least two beam portions extending from the lateral edge of the copper plate and terminating at the at least one second terminal.

15. The power semiconductor package of claim 14, wherein the at least two beam portions extend from the lateral edge of the copper plate to a cross bar portion, the cross bar portion being coupled to at least two second terminals.

16. The power semiconductor package of claim 14, further comprising a layer of curable conductive material disposed for coupling the cross bar portion to the second terminals.

17. The power semiconductor package of claim 16, wherein the curable conductive material is silver filled epoxy.



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17 18. The power semiconductor package of claim 14 15, wherein the cross bar portion includes a void located proximate to the second terminals and sized and shaped to facilitate engagement with the second terminals.

18 19. The power semiconductor package of claim 17 18, wherein the void is in the form of a channel extending substantially a length of the cross bar portion.

19 20. The power semiconductor package of claim 18 19, further comprising curable conductive material disposed within the channel to couple the cross bar portion to the second terminals.

20 21. The power semiconductor package of claim 19 20, further comprising a downwardly directed projection extending through the channel toward the second terminals.

21 22. The power semiconductor package of claim 20 21, wherein the projection is in the form of a wall extending substantially the length of the cross bar portion.

22 23. The power semiconductor package of claim 21 22, further comprising a curable conductive material disposed within the void to couple the cross bar portion to the second terminals.

23 24. The power semiconductor package of claim 22 23, wherein the curable conductive material is silver filled epoxy.

24. The power semiconductor package of claim 1, wherein the package is sized and shaped to conform to an S08 package configuration.

25. The power semiconductor package of claim 1, wherein the package includes a plastic housing which substantially encapsulates the bottom leadframe, semiconductor die and copper plate.

26. A power semiconductor package, comprising:

a bottom leadframe having a bottom plate portion and at least one first terminal extending from the bottom plate portion;

at least one second terminal being co-planar with the first terminal;

a semiconductor power MOSFET die having a top surface on which a first metalized region defining a source and a second metalized region defining a gate are disposed, the top surface further including a gate bus extending over portions of the source, the MOSFET die further including a bottom surface defining a drain connection coupled to the bottom plate of the leadframe such that the first terminal is electrically connected to the drain;

a nitride layer substantially covering at least a portion of the gate bus;

a layer of curable conductive material disposed atop the nitride layer and the source;

a copper plate coupled to and spanning a substantial part of the source and covering substantially all of the gate bus, the curable conductive material electrically coupling the copper plate to the source but

being electrically insulated from the gate bus via the nitride layer;

at least one beam portion being sized and shaped to couple the copper plate portion to the at least one second terminal such that it is electrically coupled to the source; and

a wire bond coupling the gate to a third terminal.

27. The power semiconductor package of claim 26, wherein the curable conductive material is silver filled epoxy.

28. The power semiconductor package of claim 26, wherein the at least one beam portion extends from a lateral edge of the copper plate and is coupled to the at least one second terminal at a distal end.